WHAT IS CLAIMED IS:

1. A method of describing a to-be-built integrated circuit, the method comprising:

reading first data from memory, wherein the first data corresponds to a first cell of a plurality of cells in a library used in manufacturing said integrated circuit, wherein the first data comprises a plurality of names of a corresponding plurality of signals input to the first cell; and

replacing each name in the first data with one of a plurality of new names, respectively, thereby to obtain first renamed data.

2. The method of claim 1 further comprising passing the first renamed data to a predetermined function for generating at least a first model for said first cell.

3. The method of claim 2 further comprising relating an address in a cell library of the first cell with the first model obtained after said passing.

4. The method of Claim 3 wherein said first model has a field, and the act of relating comprises:

storing said address in said field.

5. The method of claim 1 wherein after said replacing, the method further comprises replacing each of the names in the first data with one of the plurality of new names, respectively, in a second order different from a first order of said new names used to obtain the first renamed data, thereby to obtain second renamed data.

6. The method of claim 5 further comprising:

passing the first renamed data to a predetermined function for generating first model;

passing the second renamed data to said predetermined function for generating second model;

relating an address of the first cell to the first model; and

relating said address to the second model.

7. The method of Claim 1 further comprising:

repeatedly replacing each of the names in the first data with one of the plurality of new names, respectively, in an order different from a previous order used in a previous act of replacing; and

repeatedly passing renamed data obtained from said act of repeatedly replacing to said predetermined function.

8. The method of claim 1 further comprising:

reading second data from memory, wherein the second data corresponds to a second cell of the plurality of cells, wherein the second data comprises a plurality of names of a corresponding a plurality of signals input to the second cell; and

replacing each name in the second data with one of new names, respectively, thereby to obtain second renamed data.

9. The method of claim 8 further comprising:

passing the first renamed data to a predetermined function for generating first BDD or ROBDD data;

passing the second renamed data to said predetermined function for generating second BDD or ROBDD data;

relating an address of the first cell to the first BDD or ROBDD data; and

relating an address of the second cell to the second BDD or ROBDD data.

10. The method of claim 1 further comprising:

reading second data from memory, wherein the second data corresponds to a portion of a network to-be-built of interconnected circuits, wherein the second data comprises a plurality of names representing a plurality of signals input to the portion; and

replacing each name of the second data with one of a plurality of new names, respectively, thereby to obtain second renamed data.

11. The method of claim 10 further comprising:

passing the first renamed data to a predetermined function for generating first BDD or ROBDD data;

passing the second renamed data to said predetermined function for generating second BDD or ROBDD data;

comparing the first BDD or ROBDD data with the second BDD or ROBDD data within said predetermined function; and

relating the network portion to the first cell if the first BDD or ROBDD data compares equally with the second BDD or ROBDD data, respectively.

12. The method of claim 10 further comprising:

comparing the second data to a plurality of previously generated models, respectively, wherein each of the plurality of previously generated models is respectively related to one of the plurality of cells;

relating one of the plurality of cells to the network portion in response to comparing the models to the plurality of previously generated models.

13. A computer readable storage medium encoded with computer instructions to perform the reading and replacing of Claim 1.

14. A signal in a carrier medium encoded with computer instructions to perform the reading and replacing of Claim 1.

15. A method comprising:

reading first data from memory, wherein the first data corresponds to a portion of a network to-be-built of interconnected circuits, wherein the first data comprises a plurality of names representing a plurality of signals input to the portion;

replacing each name of the first data with one of a plurality of new names, respectively, thereby to obtain second renamed data.

16. The method of claim 15 further comprising:

passing the first renamed data to a predetermined function for generating BDD or ROBDD data;

the predetermined function comparing the BDD or ROBDD data to a plurality of previously generated BDD or ROBDD data, respectively, wherein each of the plurality of previously BDD or ROBDD data is respectively related to one of a plurality of cells used in manufacturing said network to be built; and

relating one of the plurality of cells to the network portion in response to comparing the BDD or ROBDD data to the plurality of previously BDD or ROBDD data.

17. A computer readable storage medium encoded with:

data related to BDD or ROBDD; and

memory address of a cell in a library of cells used in manufacturing an integrated circuit, said cell being modeled by said BDD or ROBDD.

18. The computer readable storage medium of Claim 17 wherein:

the memory address is located adjacent to the data, and accessed via a single data structure.

19. The computer readable storage medium of Claim 17 further comprising:

a table relating to the memory address.

20. A computer system comprising:

a microprocessor coupled to first and second memories;

wherein the first memory comprises a plurality of names of a corresponding a plurality of input terminals of cells of a technology library;

wherein the second memory comprises instructions executable by the microprocessor for implementing a method for replacing each name in one of the plurality of cells with one of a plurality of new names.

21. The computer system of Claim 20 wherein:

the first memory further comprises a plurality of names of input terminals of a corresponding plurality of clusters of a to-be-built electrical circuit; and

the second memory further comprises a BDD package, a first instruction to invoke the BDD package for at least one cell and a second instruction to invoke the BDD package for at least one cluster.

22. A computer readable medium storing a relationship between BDD or ROBDD data and at least one cell of a plurality of cells used in manufacturing an integrated circuit, wherein the BDD or ROBDD data was generated from data representing the at least one cell.

23. The computer readable storage medium of Claim 22 further comprising an instruction to replace each name of each input signal of each cell with a new name.

5